AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A state machine comprising:

a first input receiving a first read clock;

a second input receiving a first write clock;

a third input receiving a first programmable almost full look-ahead signal~~,~~;

a fourth input receiving a second read clock;

a fifth input receiving a second write clock; and

a sixth input receiving a second programmable almost full look-ahead signal, wherein said state machine ~~manipulating said inputs to produce~~ is configured to generate an output signal representing an almost full output flag that is at a first logic state when a FIFO is almost full and is at a second logic state when said FIFO is not almost full in response to said first read clock, said first write clock, said first programmable almost full look-ahead signal, said second read clock, said second write clock and said second programmable almost full look-ahead signal.

2. (CURRENTLY AMENDED) An apparatus comprising:

a first set state machine ~~having a first input receiving a first read clock, a second input receiving a first write clock, a third input receiving a first programmable almost full look-ahead~~

~~signal, and a fourth input to receive a first control signal, said first set state machine manipulating said inputs to produce~~ configured to generate a first set-output signal that is either at a first logic state or at a second logic state in response to (i) a first read clock, (ii) a first write clock, (iii) a first programmable almost full look-ahead signal and (iv) a first control signal;

a second set state machine ~~having a first input receiving a second read clock, a second input receiving a second write clock, a third input receiving a second programmable almost full look-ahead signal, and a fourth input to receive a second control signal; said second set state machine manipulating said inputs to produce~~ configured to generate a second ~~set_output~~ set-output signal that is either at said first logic state or at said second logic state in response to (i) a second read clock, (ii) a second write clock, (iii) a second programmable almost full look-ahead signal and (iv) a second control signal;

a synchronizer ~~coupled to said second set state machine, said synchronizer receiving said second set_output signal and receiving a reset signal; said synchronizer~~ configured to generate a synchronized output signal in response to said second set-output signal and a reset signal;

a latch ~~having a first input receiving said first set_output signal, a second input receiving said synchronized~~

~~output signal, a first latch_output presenting said first set_output signal as a first latch_output signal, and a second latch_output presenting said synchronized output signal as a second latch_output signal, said latch being configured to hold said first latch_output signal and said second latch_output signal until said first set_output signal and second set_output signal change logic states~~ configured to generate (i) a first latch output signal in response to said first set-output signal and said synchronized output signal and (ii) a second latch output signal as a complement of said first latch-output signal, said first ~~latch_output~~ latch output signal representing an almost full output flag that is at ~~a~~ said first logic state when a FIFO (First In First Out) memory block is almost full, and is at ~~a~~ said second logic state when said FIFO is not almost full~~; said second latch_output signal representing said not almost full output flag that is at said first logic state when said FIFO is not almost full and is at said second logic state when said FIFO is almost full~~;

a first logic block ~~having a logic input receiving said second latch_output signal, and a logic output presenting said second latch_output signal as~~ configured to generate said first control signal ~~to said first set state machine~~ in response to said second latch output signal; and

a second logic block ~~having a logic input receiving said first latch_output signal, a first logic output presenting said~~

~~first latch_output signal as said second control signal to said second set state machine, and a second logic output presenting said first latch_output signal as~~ configured to generate (i) said reset signal and (ii) said second control signal in response to said first latch output signal ~~to said synchronizer~~.

3. (CURRENTLY AMENDED) The apparatus of claim 2, wherein said synchronizer ~~further includes~~ comprises:

a SR latch ~~coupled to said second set state machine, said SR latch configured to receive said second set_output signal from said second set state machine, configured to receive said reset signal from said second logic block, and~~ configured to time ~~an output of~~ said second ~~set_output~~ set-output signal depending on said reset signal; and

a Flip-Flop (FF) block ~~coupled to said SR latch, said FF configured to receive said second set_output signal, and configured to time the presentation of said second set_output signal as~~ configured to generate said synchronized signal depending on (i) an external timing signal and (ii) said second set-output signal as timed by said SR latch.

4. (CURRENTLY AMENDED) The apparatus of claim 3, wherein said external timing signal ~~further~~ comprises:

a free running write clock signal.

5. (ORIGINAL) The apparatus of claim 2, wherein said FIFO comprises:

a synchronous FIFO.

6. (CURRENTLY AMENDED) The apparatus of claim 2, wherein said first write clock ~~further~~ comprises:

a first enabled write clock.

7. (CURRENTLY AMENDED) The apparatus of claim 2, wherein said first read clock ~~further~~ comprises:

a first enabled read clock.

8. (CURRENTLY AMENDED) The apparatus of claim 2, wherein said second write clock ~~further~~ comprises:

a second enabled write clock.

9. (CURRENTLY AMENDED) The apparatus of claim 2, wherein said second read clock ~~further~~ comprises:

a second enabled read clock.

10. (CURRENTLY AMENDED) The apparatus of claim 2 further comprising:

a first delay block configured to ~~provide a first predetermined delay to said first set_output signal in order to~~

increase a first pulse width of said first ~~set_output~~ latch output signal before said second logic block.

11. (CURRENTLY AMENDED) The apparatus of claim ~~2~~ 10 further comprising:

a second delay block configured to ~~provide a second predetermined delay to said second set_output signal in order to~~ increase a second pulse width of said second ~~set_output~~ latch output signal before said first logic block.

12. (CURRENTLY AMENDED) The apparatus of claim 10, wherein said first delay block ~~further includes:~~

~~a first predetermined delay block having~~ has a ~~first~~ predetermined delay configured during fabrication.

13. (CURRENTLY AMENDED) The apparatus of claim 10, wherein said first delay block ~~further includes~~ comprises:

a ~~first~~ programmable delay block configured to change ~~a~~ said first pulse width ~~of said first set_output signal~~.

14. (CURRENTLY AMENDED) The apparatus of claim 10, wherein said first delay block ~~further includes~~ comprises:

a ~~first~~ programmable delay block responsive to an externally generated signal.

15. (CURRENTLY AMENDED) The apparatus of claim 14, wherein said ~~first~~ programmable delay block ~~further~~ comprises:

a joint test access group (JTAG) ~~first~~ programmable delay block.

16. (CURRENTLY AMENDED) The apparatus of claim ~~14~~ 15, wherein ~~said first programmable delay block further comprises:~~

~~a joint test access group (JTAG) first programmable delay block, wherein the existing JTAG input ports including~~ a set of additional JTAG instructions are utilized to program said JTAG programmable delay block ~~delay line~~.

17. (CURRENTLY AMENDED) The apparatus of claim 11, wherein said second delay block ~~further includes:~~

~~a second predetermined delay block having~~ has a second predetermined delay configured during fabrication.

18. (CURRENTLY AMENDED) The apparatus of claim 11, wherein said second delay block ~~further includes~~ comprises:

a ~~second~~ programmable delay block configured to change ~~a~~ said second pulse width ~~of said second set output signal~~.

19. (CURRENTLY AMENDED) The apparatus of claim 11, wherein said second delay block ~~further includes~~ comprises:

a ~~second~~ programmable delay block responsive to an externally generated signal.

20. (CURRENTLY AMENDED) The apparatus of claim 19, wherein said ~~second~~ programmable delay block further comprises:

a joint test access group (JTAG) ~~second~~ programmable delay block.

21. (CURRENTLY AMENDED) The apparatus of claim ~~19~~ 20, wherein ~~said second programmable delay block further comprises:~~

~~a joint test access group (JTAG) second programmable delay block, wherein the existing JTAG input ports including~~ a set of additional JTAG instructions are utilized to program said JTAG programmable delay block ~~delay line~~.

22. (CURRENTLY AMENDED) A method for determining ~~the~~ an almost emptiness of at least one memory buffer, comprising the steps of:

(A) generating ~~at least one~~ an almost full output flag in response to ~~a plurality of signals comprising:~~ (i) a first read clock, (ii) a first write clock, (iii) a first programmable almost full look-ahead signal, (iv) a second read clock, (v) a second write clock~~,~~ (vi) and a second programmable almost full look-ahead signal;

(B) generating ~~at least one~~ a not almost full output flag as a complement of said almost full output flag ~~in response to a plurality of signals comprising: a first read clock, a first write clock, a first programmable almost full look-ahead signal, a second read clock, a second write clock, and a second programmable almost full look-ahead signal~~; and

(C) presenting said first read clock, said first write clock, said first programmable almost full look-ahead signal, said second read clock, said second write clock~~,~~ and said second programmable almost full look-ahead signal to a state machine, wherein said state machine generates said ~~at least one~~ almost full output flag and said ~~at least one~~ not almost full output flag.

23. (CURRENTLY AMENDED) The method of claim 22, wherein said step of generating said ~~at least one~~ almost full output flag ~~further includes the step~~ comprises the sub-step of:

delaying said step of generation of said ~~at least one~~ almost full output flag by a time delay.

24. (CURRENTLY AMENDED) The method of claim 22, wherein said step of generating said ~~at least one~~ not almost full output flag ~~further includes the step~~ comprises the sub-step of:

delaying said step of generation of said ~~at least one~~ not almost full output flag by a time delay.

25. (CURRENTLY AMENDED) The method of claim 22, wherein said step of generating said ~~at least one~~ almost full output flag ~~further includes the steps~~ comprises the sub-steps of:

programming a time delay; and

delaying said step of generation of said ~~at least one~~ almost full output flag by said ~~programable~~ time delay.

26. (CURRENTLY AMENDED) The method of claim 22, wherein said step of generating said ~~at least one~~ not almost full output flag ~~further includes the steps~~ comprises the sub-steps of:

programming a time delay; and

delaying said step of generation of said ~~at least one~~ not almost full output flag by said ~~programable~~ time delay.

27. (CURRENTLY AMENDED) The method of claim 22, wherein said step of generating said ~~at least one~~ almost full output flag ~~further includes the steps~~ comprises the sub-steps of:

using JTAG to program a programable time delay; and

delaying said step of generation of said ~~at least one~~ almost full output flag by said ~~JTAG~~ programable time delay.

28. (CURRENTLY AMENDED) The method of claim 22, wherein said step of generating said ~~at least one~~ not almost full output flag ~~further includes the steps~~ comprises the sub-steps of:

using JTAG to program a programable time delay; and

delaying said step of generation of said ~~at least one~~ not almost full output flag by said ~~JTAG~~ programable time delay.

29. (CURRENTLY AMENDED) An apparatus comprising:

~~a first manipulating~~ means for ~~receiving a first plurality of input signals comprising: a first read clock, a first write clock, a first programmable almost full look-ahead signal, and a first control signal; said first means manipulating said first plurality of input signals to produce~~ generating a first output signal ~~that is~~ either at a first logic state or at a second logic state in response to (i) a first read clock, (ii) a first write clock, (iii) a first programmable almost full look-ahead signal and (iv) a first control signal;

~~a second manipulating~~ means for ~~receiving a second plurality of input signals comprising: a second read clock, a second write clock, a second programmable almost full look-ahead signal, and a second control signal; said second means manipulating said second plurality of input signals to produce~~ generating a second output signal ~~that is~~ either at ~~a~~ said first logic state or at ~~a~~ said second logic state in response to (i) a second read

clock, (ii) a second write clock, (iii) a second programmable almost full look-ahead signal and (iv) a second control signal;

~~a synchronizer~~ means for ~~synchronizing said first output signal and said second output signal, said synchronizer means configured to receive said second output signal and configured to receive a reset signal, said synchronizer means configured to generate~~ generating a synchronized output signal in response to (i) said second output signal and (ii) a reset signal;

~~a latch~~ means for ~~configured to receive said first set_output signal, and said synchronized output signal, said latch means configured to present said first output signal as a first latch_output signal, and said synchronized output signal as a second latch_output signal, said first latch_output~~ generating (i) a first latch output signal representing an almost full output flag that is at a first logic state when a FIFO memory block is almost full, and is at a second logic state when said FIFO is not almost full~~, said~~ and (ii) a second latch output signal as a complement of said first latch output signal ~~representing said not almost full output flag that is at said first logic state when said FIFO is not almost full and is at said second logic state when said FIFO is almost full~~;

~~a first logic~~ means for ~~configured to receive said second latch_output signal, and configured to present said second latch_output signal as a~~ generating said first control signal in

response to said second latch output signal ~~to said first manipulating means~~; and

~~a second logic~~ means for ~~configured to receive said first latch_output signal, configured to present said first latch_output signal as~~ generating (i) said second control signal ~~to said second manipulating means, and configured to present said first latch_output signal as~~ and (ii) said reset signal in response to said first latch output signal ~~to said synchronizer means~~.

30. (CURRENTLY AMENDED) The apparatus of claim 29 further comprising:

~~a first delay~~ means for ~~configured to provide a first delay to said first output signal in order to increase~~ increasing a pulse width of said first latch output signal.

31. (CURRENTLY AMENDED) The apparatus of claim 29 further comprising:

~~a second delay~~ means for ~~configured to provide a second delay to said second output signal in order to increase~~ increasing a pulse width of said second latch output signal.